We Claim:

1. A memory configuration, comprising:

at least two semiconductor memory modules, including a first semiconductor memory module and a second semiconductor memory module, controlled by internal clock signals, said two semiconductor memory modules output or receive data only on one of a rising edge and a falling edge;

an interface device for receiving an external clock signal and the data on a rising edge and a directly succeeding falling edge of the external clock signal or outputs the data between the rising edge and the directly succeeding falling edge of the external clock signal; and

a conversion device connected between said interface device and said two semiconductor memory modules to route the data for outputting or reception.

2. The memory configuration according to claim 1, wherein the external clock signal is fed to said interface device and, said the conversion device generates complementary clock signals, of which one of the complementary clock signals is fed to said first semiconductor memory module and another of the complementary clock signals is fed to said second semiconductor memory module.

3. The memory configuration according to claim 2, wherein said conversion device has a delay locked loop with an input side receiving the external clock signal and an output side outputting the complementary clock signals functioning as the internal clock signals, said delay locked loop connected to said interface device.

4. The memory configuration according to claim 1, wherein said conversion device has a command decoder for detecting a command for receiving data, the command for receiving data contains at least two signal pulses present on the rising edge of the external clock signal, and in that the command for receiving data is forwarded to said first semiconductor memory module in a manner delayed by 3 ½ clock periods of the external clock signal and is forwarded to said second semiconductor memory module in a manner delayed by three clock periods of the external clock signal.

5. The memory configuration according to claim 1, wherein said command decoder detects a command for outputting data, the command for outputting data contains two signal pulses present on the rising edge of the external clock signal, and the command for outputting data is forwarded to said first semiconductor memory module in a manner delayed at most by one clock cycle of the external clock signal and is forwarded to

said second semiconductor memory module in a manner delayed at most by 1 ½ clock periods of the external clock signal.

6. The memory configuration according to claim 4, wherein the command for receiving data contains the two signal pulses that each have a low level and are centered with respect to two rising edges of the external clock signal that are separated by two clock periods.

7. The memory configuration according to claim 2, wherein:

said first semiconductor memory module has a data signal terminal;

said second semiconductor memory module has a data signal terminal; and

said conversion device has a changeover switch with a first terminal connected to said interface device, a second terminal connected to said data signal terminal of said first semiconductor memory module, and a third terminal connected to said data signal terminal of said second semiconductor memory module, said changeover switch able to switch over between said second terminal and said third terminal, and in that a driving of said changeover switch can be controlled in

a manner dependent on each edge change of the external clock signal.

8. The memory configuration according to claim 7, wherein

said interface device has a data signal terminal; and

a first data value to be output or input at said first semiconductor memory module and a second data value to be output or input at said second semiconductor memory module are alternately present at said data signal terminal of said interface device after every half clock period of the external clock signal.

9. The memory configuration according to claim 1, wherein said conversion device contains a signal generator for generating a clock signal whose edges are oriented to edges of a data signal during a data outputting and which has edges which are oriented to a binary signal level of the data signal during a data inputting.

10. The memory configuration according to claim 1, wherein said conversion device has at least two further memory modules for storing a respective further bit of a data word, one of said further memory modules is connected in parallel with said first semiconductor memory module and another of said further

memory modules is connected in parallel with said second semiconductor memory module.

11. The memory configuration according to claim 5, wherein the command for outputting data contains the two signal pulses that each have a low level and are centered with respect to two rising edges of the external clock signal which are separated by two clock periods.